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THESIS

DESIGN AND TESTING OF AN OPTICAL DIGITAL LINK CAPABLE OF 14-CHANNEL TRANSMISSION

by

Nejat Polat

September 1994

Thesis Advisor: John P. Powers

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Design and Testing of An Optical Digital Link Capable of
14-Channel Transmission

by

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Submitted in partial fulfillment
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ABSTRACT

This thesis presents the design, implementation and evaluation of a communication system, capable of serializing 14-channel digital parallel data, transmission and reception of the serial data over a high speed fiber link at 39 Mbps and converting the serial data back to its 14-channel parallel form. A time division multiplexing technique was used to transmit the data. The high-speed Emitter-Coupled Logic devices were employed to construct the design.

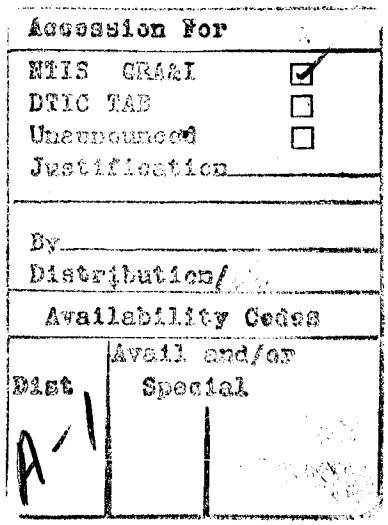

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

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I would like to express my sincere gratitude to my country and the Turkish Navy for giving me opportunity to make this study.

I. INTRODUCTION

A. GENERAL CONCEPT OF THE THESIS

This thesis is a continuation of ongoing research being conducted at the Naval Postgraduate School involving the development of an RF analog-to-digital (A/D) converter and a high-speed fiber-optic communication link. The RF signal is received by an RF-antenna and converted to 14-channel parallel data with an electro-optic analog-to-digital converter at the antenna mask. (See Fig 1.1.) The outputs of the converter are connected to an optical transmitter, which serializes the data and transmits the serial data to an optical receiver below the deck through a high-speed fiber link. The optical receiver converts the data back to 14-channel parallel data word and sends it to the signal processing units.

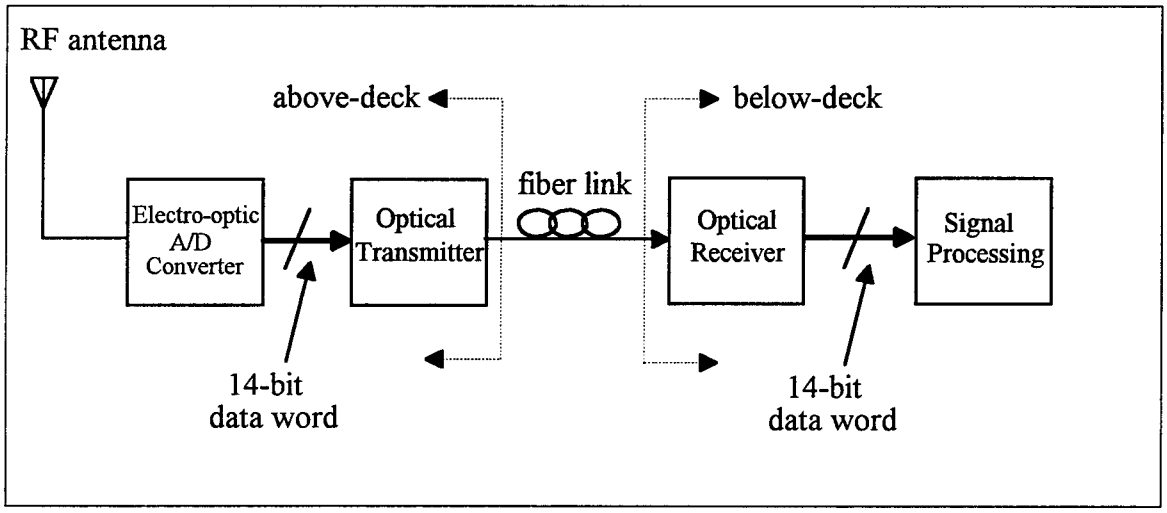


Figure 1.1. Simplified Block Diagram of the RF Receiver System.

The particular subject of this thesis was to design, construct and test the transmitter and the receiver system capable of:

a) serializing the 14-bit digital parallel data,

b) transmitting and receiving the data over an electrical wire link and

c) converting the serial data back into a 14-bit parallel data word.

The parallel data are converted to a serial data by the use of a special parallel-to-serial converter. The serial data are transmitted through a wire link with a design bit rate of 70 Mbps (see Fig. 1.2). At the other end of the link, the receiver receives and converts the serial data back to parallel form with a serial-to-parallel converter.

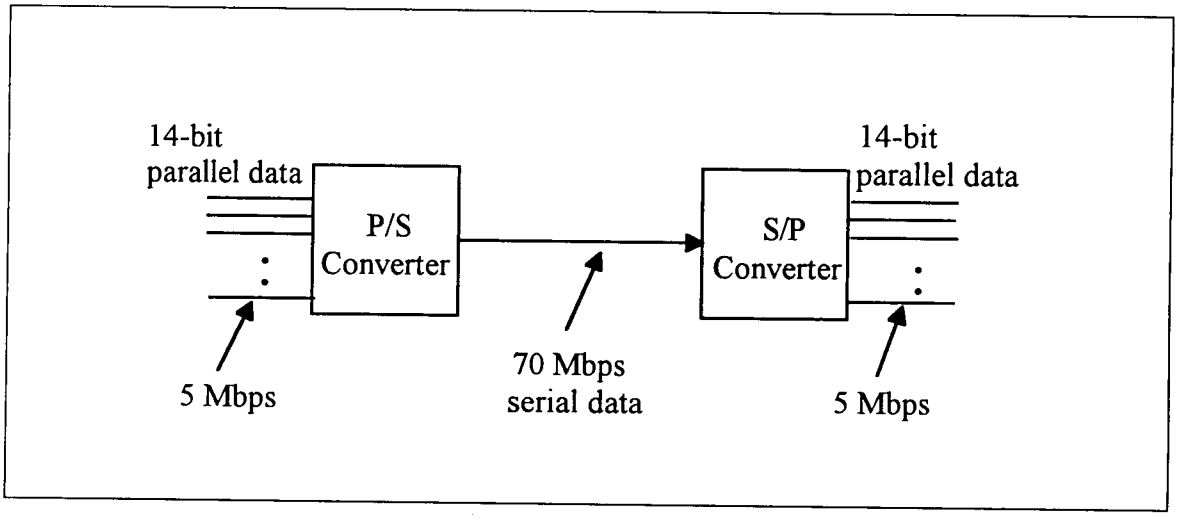


Figure 1.2. Simplified Block Diagram of the Transmitter-Receiver System.

The optical transmission of the data over a high speed optical link will not be examined in this thesis. But the ultimate data transmission will occur over an optical link, as shown in Fig. 1.3. The serial data from the transmitter modulates the optical source, which is then introduced to a fiber link. At the receiver end of the link, an optical detector

receives and retrieves the serial data. The serial data is ultimately converted back to parallel form with a serial-to-parallel converter.

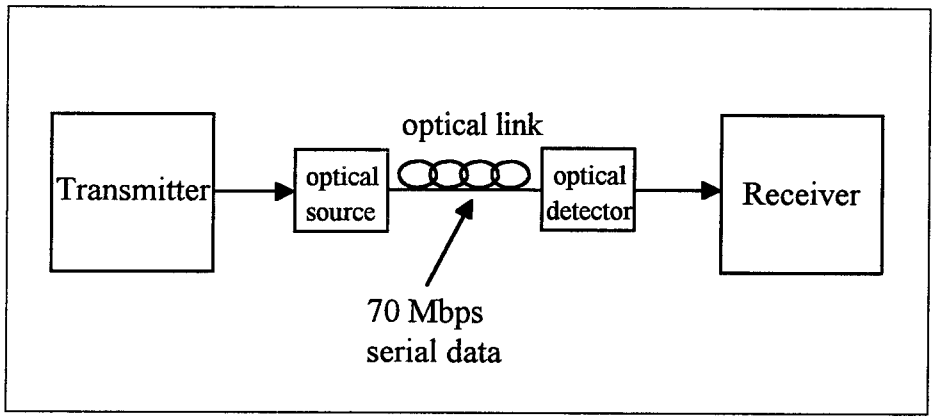


Figure 1.3. The Optical Transmission of the Data

B. REQUIREMENTS

In addition to the data transmission line, two other links between the transmitter and the receiver need to be used to guarantee the correct data reception, as will be discussed in detail later in Sections II.A and IV.C. These links are the clock signal and a sync pulse (see Fig. 1.4). However, there are some techniques to embed the clock and the sync pulse into the same link with data, but the overhead of this is to increase the bit rate in the serial data channel.

The reader will appreciate that the high speed data rate which is used in this thesis forces the use of "Emitter-Coupled Logic" in the circuit design. ECL is today's fastest form of silicon-based digital logic. The high speed rise times, low propagation delays and very short setup/hold time of the ECL devices make them very suitable for high speed,

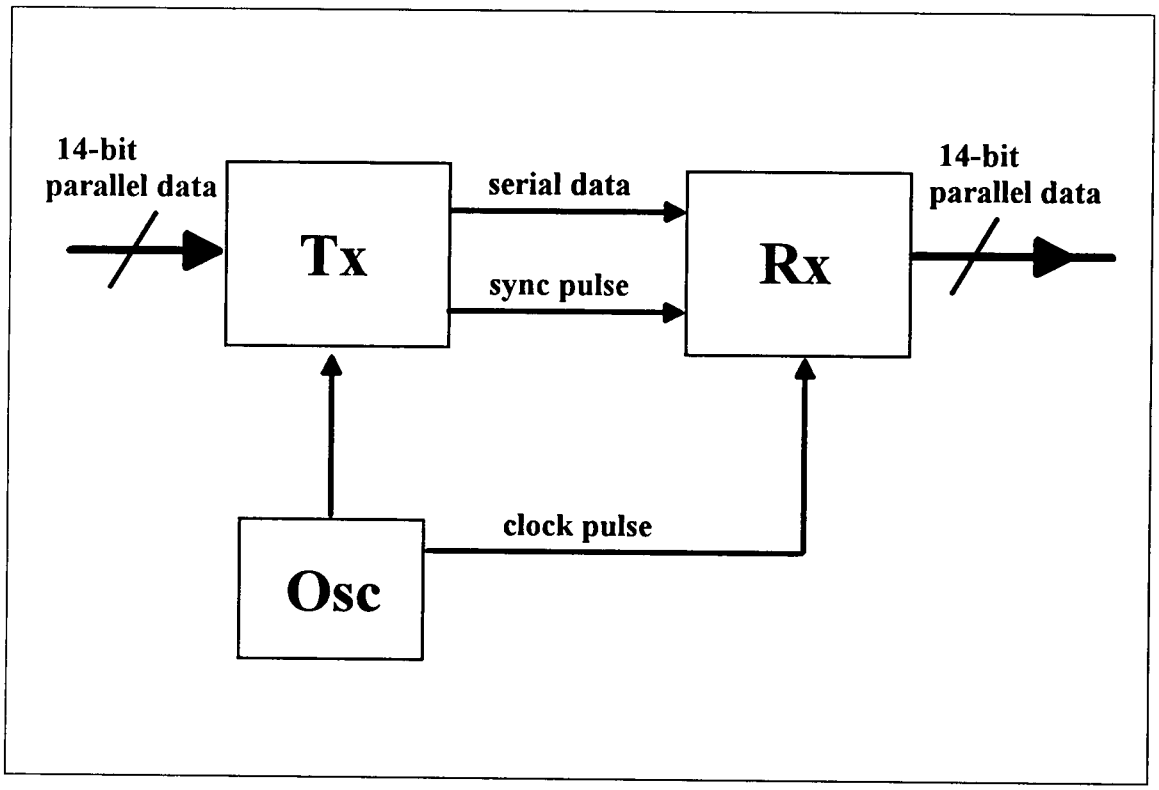


Figure 1.4. Links Between Transmitter and Receiver.

high frequency logic design. The saturated logic families, such as TTL, do not meet the requirements for a high frequency logic design.

A crystal oscillator was used to generate a 70 MHz clock which provides a signal that is free from noise. The integrated circuit oscillators of the ECL family have very fast edge speeds which cause distortion due to reflections on signal lines. This feature requires utilization of some special interconnection and wiring techniques, which limit the flexibility of the implementation. Our application does not require such fast edge speeds, so a crystal oscillator, which provides a signal which has a somewhat slower edge speed but is free from distortion, is a better choice for this thesis design.

C. MULTIPLEXING TECHNIQUES

Multiplexing is a technique to share a single data link among multiple data channels. As depicted in Fig. 1.5, *n* inputs are accepted by the multiplexer and combined into a single high-capacity data link. The demultiplexer at the other side receives the data stream, separates the multiple data channels and delivers them to the appropriate output lines.

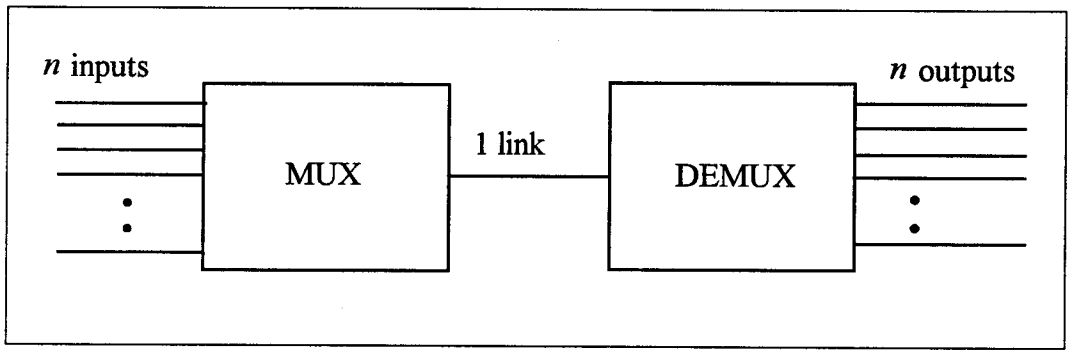


Figure 1.5. Multiplexing and Demultiplexing

Multiplexing techniques can include:

- time-division multiplexing (TDM),
- frequency-division multiplexing (FDM),
- code-division multiple-access multiplexing (CDMA) and
- wavelength-division multiplexing (WDM).

TDM assigns different time intervals to the individual signals and transfers them to the transmission link one-by-one in physically different time intervals. The same frequency and the same coding/modulating technique can be used for all signals. This was the technique used in this thesis.

FDM assigns different frequency segments to each signal. The individual signals to be transmitted are modulated with different carrier frequencies. The signals are then summed and transmitted simultaneously over the same communication channel. Each signal is allocated distinct segments of the frequency band. The demultiplexer extracts the signals with the use of different bandpass filters. Commercial radio and television stations use this technique.

In CDMA, the different signals share the same frequency band simultaneously in time. Each signal is coded with a different code; in other words, they are assigned a particular digitally encoded waveform that is orthogonal to the others. This technique is currently under investigation in cellular telephone and in fiber optics.

WDM is mainly employed with fiber-optic links. Since optical fibers have broad region of low loss that can support the operation with more than one source, it is possible

to transmit the data with different emitters having different operating wavelengths. The couplers (multiplexers) at the transmitter end combine the separate source emissions. At the receiver, filters or other wavelength-sensitive elements, separate the wavelengths to separate receivers for detection.

TDM is to be used when the bandwidth of the transmission medium does not allow the transmission of multiple signals with high data rate by using distinct frequency band allocation. For this thesis design, TDM technique was employed for data transmission, since 14-separate parallel data are to be transmitted with a high bit rate.

D. SYSTEM DESIGN OVERVIEW

Figures 1.2 and 1.4 show a simplified block diagram of the transmitter receiver system. Chapter II discusses the operation of the transmitter briefly, followed by a detailed description of the circuit. Chapter III describes the receiver in the same manner. Chapter IV presents the test procedures and the problems experienced throughout the evaluation process. Finally Chapter V contains some final remarks and recommendations for areas of further study.

II. TRANSMITTER

A. OVERVIEW

The basic goal of the transmitter was to serialize the 14-channel high speed digital data operating at 5 megawords per second into a single channel and to transmit the data at 70 Mbps through an optical link. Conceptually, other links would be used to transmit the clock signal and sync pulse signal which provides synchronization between transmitter and receiver. In our experiment these signals were transmitted by wire to the receiver.

Figure 2.1 is a simplified functional schematic of the transmitter. The main components of the transmitter are:

- a 14-bit buffer,
- a 14-bit multiplexer,
- a counter and
- control logic (sync pulse generator).

Before discussion of each module in detail, a general overview of the transmitter will be presented here.

The bit-rate of the incoming digital data is assumed not to exceed 5 Mbps (in each channel) for this design. This provides a period of 200 ns ($=1/5x10^6$). To send 14 separate digital data bits in one period requires a bit-rate of 70 Mbps. The first step of transmitting the 14-bit parallel data is the input of the buffer. A buffer is a device that transfers the data present at its input to the output when triggered with a clock pulse. Any change of the

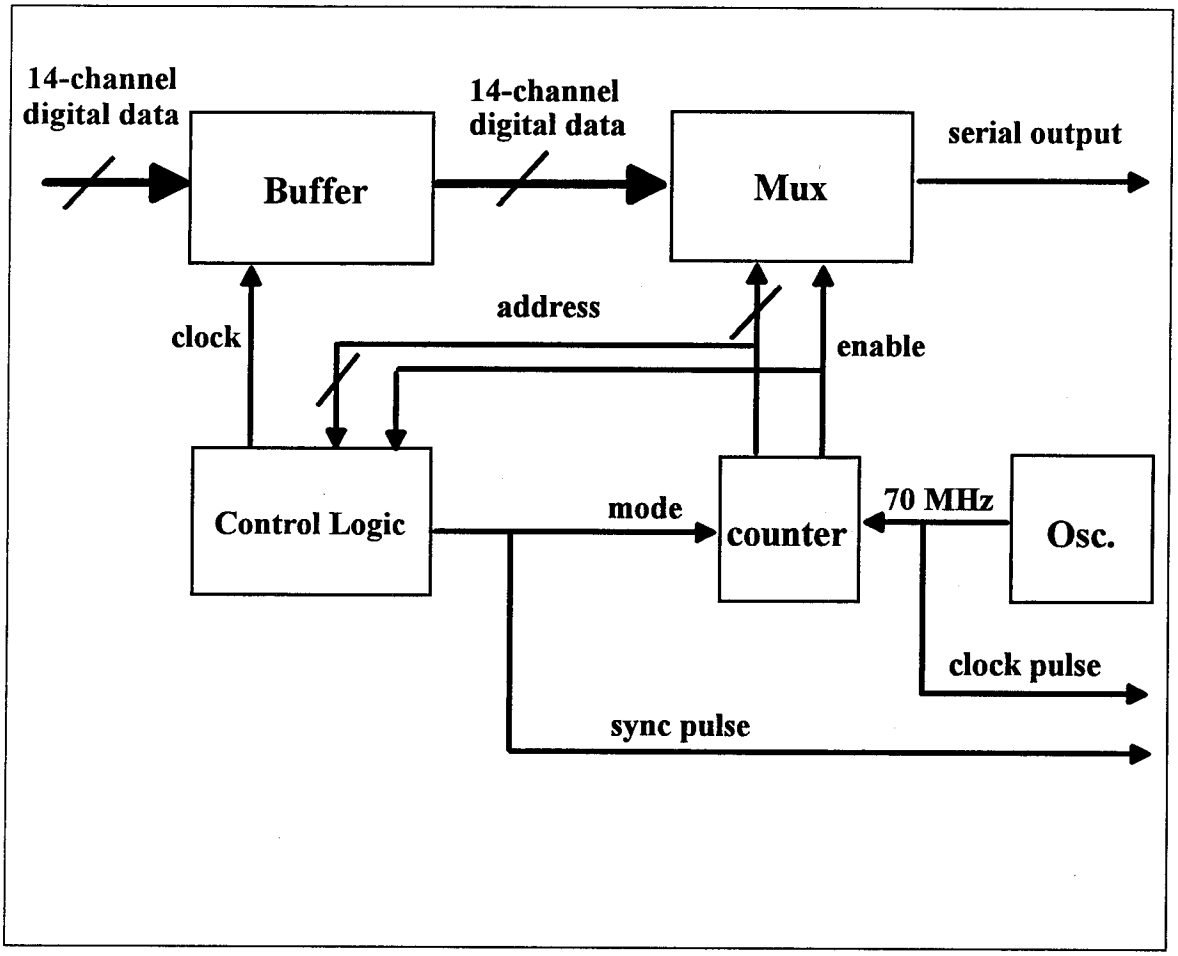


Figure 2.1. Functional Schematic of the Transmitter.

data at the input does not affect the output any other time. (The buffer acts as a sample-and-hold circuit.) The buffer sampling function is activated by a trigger pulse and it samples the input data. The buffer then transfers the data values to the output and holds the voltage levels at its output constant, which provides a stable data output until the next trigger pulse.

The parallel outputs of the buffer are connected to the inputs of the multiplexer (Mux) via 14 separate channels. The multiplexer selects one of the inputs (according to the code present on the address inputs) and routes the input value to the output. For this design, the address inputs of the multiplexer are sequentially generated by a counter in the 200 ns period. Since the data coming from the buffer are stable for 200 ns, the multiplexer will transfer the 14-channel parallel inputs to the output one-by-one. The cycle repeats itself every 200 ns.

A stable crystal oscillator with a frequency of 70 MHz provides a trigger pulse for the counter. This pulse was also transmitted to the receiver with a separate wire link. Although another 70 MHz clock pulse could be generated with a separate crystal by the receiver, it is not possible to generate exactly the same frequency and to trigger at the same time. This asynchronous operation generates data errors. Hence we need another link between transmitter and receiver for the clock which is undesirable. There are some techniques to send the clock pulse with the digital data on the same channel which is beyond the scope of this thesis. The drawback of encoding the clock in the data is the

requirement to double the signal data rate of the fiber channel to 140 Mbps and the resultant need for clock signals of that speed.

The control logic block of Fig. 2.1 controls the operation mode of the counter which is either "increment" or "parallel entry". When the counter is in the "increment" mode, its address outputs are incremented by a binary "1" starting from "0000" with every clock pulse. The "parallel entry" mode provides the counter to load 4-bit address information at its parallel inputs to the address outputs. The control logic also generates a synchronization pulse every 200 ns to synchronize the receiver with the transmitter.

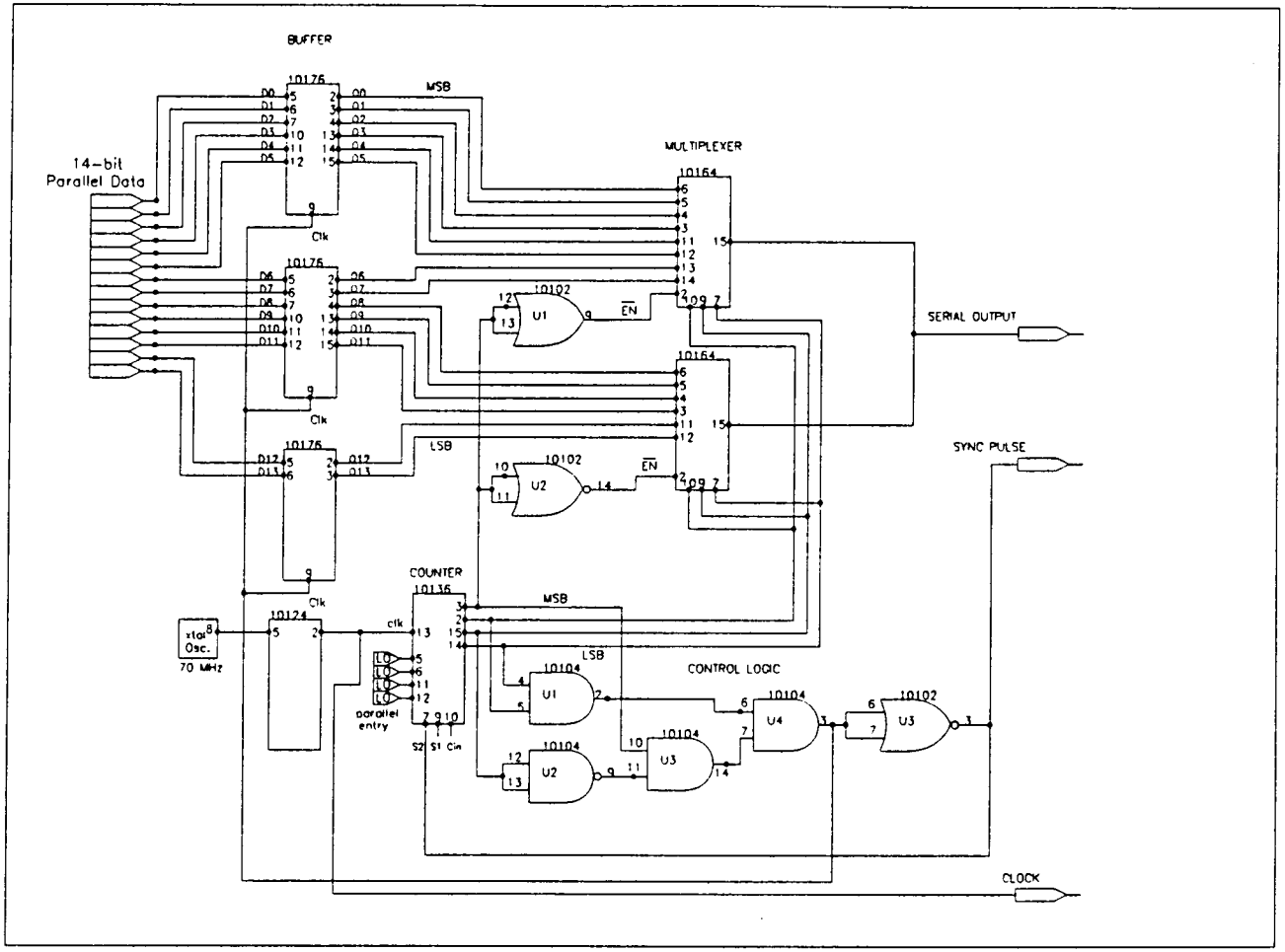
The outputs from the transmitter are:

- the serial data output,
- the sync pulse and
- the 70 MHz clock sequence.

With this overview of the transmitter circuitry in mind, each module will now be examined in detail. The detailed circuit is shown in Fig. 2.2.

B. 14-BIT BUFFER

The first circuit for the incoming data is a buffer composed of 14 high-speed, master-slave, type "D" flip-flops contained in three 10176 ECL chips (the left-most devices in Fig. 2.2). Four of the flip-flops in the last chip were not used. The buffer, acting as a sample-and-hold circuit, provides stable data outputs during a period of 200 ns which are the inputs to the multiplexer. The data transfer to the outputs takes place on the positive-going clock transition having a frequency of 5 MHz. Any change in input data



*pull-down resistors are not shown for convenience

Figure 2.2. Transmitter Circuit

after the transfer will not affect the output until a new clock pulse is received, at which time this new input data are transferred to the output of the buffer. A toggle frequency of 150 MHz and a maximum rise/fall time of 4 ns make the flip-flops convenient for high speed data.

When the last bit of data is being sent through the output channel of the transmitter, a trigger pulse is generated by the control logic circuit which triggers the buffer to receive the new input data samples.

C. MULTIPLEXERS

The outputs of the buffer are directly connected to the input of the multiplexers (the 10164 devices in Fig. 2.2). The data are continuously present at the input of the multiplexers except during settling time of the buffer. (The settling time is the time for the output of the buffer to become stable after clock pulse is received.)

The first multiplexer (the upper 10164 device in Fig. 2.2) is enabled for the first eight bits of the data by the most significant bit of the counter while the second one (the lower 10164 device in Fig. 2.2) is disabled at the time. For the last six bits of the data, the second multiplexer will be enabled. Since the enable/disable signal is common for the two multiplexers, an inverter is used for the second one. The inverter is a simple NOR-gate (U2-10102 in Fig. 2.2) whose inputs are tied together. To avoid timing problems between the two multiplexers in accordance with the enable/disable signal, an OR-gate of the same type is used in front of the enable input of the first multiplexer (U1-10102 in Fig. 2.2). This introduces an equal delay time. (Otherwise, a short low level spike occurs at the

output after first multiplexer is disabled until the second one is enabled. The pulse width of the spike equals the propagation delay of the NOR-gate.) The inputs of the OR-gate are tied together as well. The address inputs of the multiplexers choose which input will be sent to the output. That address information is generated with a hex counter. (See next section).

The ECL logic family permits direct connections of the outputs (which is called wire-OR connections). So, the outputs of the multiplexers are connected together making a single multiplexer output. When one of the multiplexers is disabled, its output will be low which will make the output channel the same as the output of the other multiplexer.

D. COUNTER

The counter is basically a high-speed synchronous hexadecimal counter (the 10136 device in Fig. 2.2). The 70 MHz crystal oscillator provides a stable, noiseless clock pulse for the counter. It is an important issue to use a crystal oscillator, because noise is the major problem for the ECL family. Very steep leading and trailing edges (fast rise and fall times) of the high-speed signals are rich in harmonics. The crystal, however, provides a somewhat slowed rise and fall time which is free from harmonics. Since the crystal oscillator generates a TTL logic level output, the signal needs to be converted to an ECL logic level. For this purpose, a TTL-to-MECL translator, shown as 10124 in Fig. 2.2, is used. The output of the translator is then fed into the counter.

The operating mode of the counter is determined by the logic circuit via control inputs (S1, S2 and Cin). The "S1" and "Cin" inputs are at logic "0" level all the time. The

"S2" input is connected to the control logic. (For operating modes of the counter, see Fig. 2.3). When "S2" is at logic "1", the counter starts counting up from "0000". The most significant bit enables the first multiplexer and disables the second. When "1000" is reached, the second multiplexer is enabled and starts sending the data to the output. When "1101" is reached, which means the last bit is being sent, the "S2" input of the counter goes low and the counter enters into the "parallel entry" mode. The very next clock pulse initializes the counter again.

S1	S2	Cin	Operating mode
L	L	ϕ	Parallel entry (program)
L	H	L	Increment (count up)
L	H	H	Hold count
H	L	L	Decrement (count down)
H	L	H	Hold count
H	H	ϕ	Hold count

ϕ : don't care

Figure 2.3. The Operating Modes of the Counter.

E. CONTROL LOGIC

The control logic circuit controls the operation of the other modules and the receiver as well. (See the lower 10102 and 10104 gates in Fig. 2.2).

The control logic provides three functions:

- it controls the operation of the counter,
- it generates the sync pulse for the receiver and
- it triggers the buffer for the new data.

When the counter reaches "1101", which is the terminal count, the second multiplexer sends the last bit of the data. At that time, the control logic generates a low level pulse. The duration of the pulse is one period of the clock. This low-level pulse causes the counter to enter into "parallel entry" mode. The next clock pulse resets the counter to "0000" and the control signal goes high again.

The same low-level pulse is also used to synchronize the receiver with the transmitter. The receiver should receive the low-level pulse one clock-period later than the counter in order to catch the last bit of the information. The propagation delays of the logic circuit and the NOR-gates in the receiver provides this delay. So, the sync pulse arrives at the receiver one period later.

The control logic also generates a clock pulse for the buffers which triggers the buffer when the counter reaches terminal count.

F. SUMMARY

In this chapter, the general concepts of the transmitter have been introduced in the first section. (Fig. 2.1.) Other sections have given the reader more detailed discussion of the circuit. (Fig. 2.2.) The next chapter will focus on the receiver in the same manner. First a general overview of the receiver will be given, followed by a detailed discussion of the circuit.

III. RECEIVER

A. OVERVIEW

In this chapter, a general overview of the receiver will be introduced to the reader which is followed by a detailed description of the schematic diagram. Some timing problems that occurred during test procedures will be discussed in Chapter IV.

The purpose of the receiver is to receive the serial data coming from the transmitter and to convert it back to 14-channel parallel form. The receiver is composed of a shift register, a buffer and a delay circuit (see Fig. 3.1).

The serial data streaming to the receiver are accepted by the shift register. A shift register is a device capable of shifting the data present at its serial input to the parallel outputs with a clock pulse. The control inputs of the shift register determine the operation modes. The specifications of the shift register specifically used in the receiver are given in Appendix A.

The sync pulse from the transmitter initializes the cycle of the shift register. The serial data are loaded sequentially to the parallel outputs until the next sync pulse. When the "data ready strobe" appears on the "data ready line" of the shift register, the buffer in the receiver is triggered and the data are transferred to the output of the buffer (for the operation of a buffer, refer to Section II.A). This is the final output of the system. The delay circuits are used to adjust the arriving time of the sync pulse at the shift register and

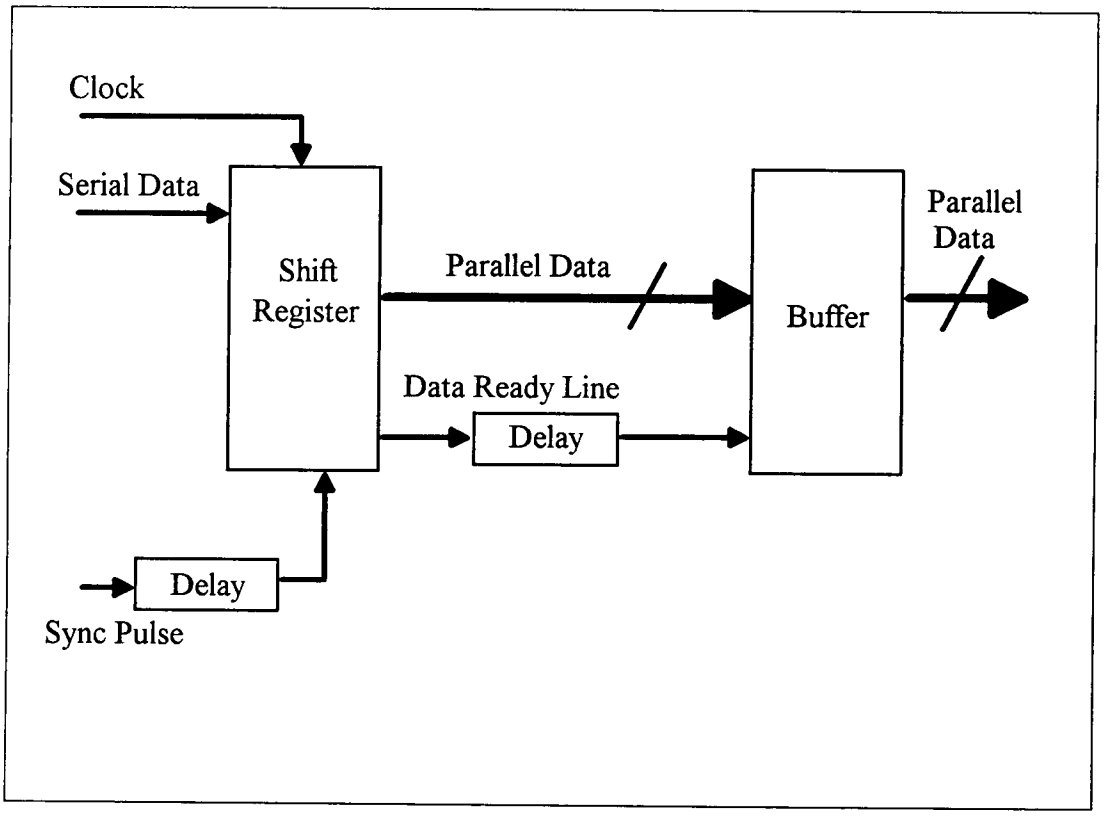


Figure 3.1. Functional Schematic of the Receiver

to provide enough "data setup time" for the buffer. The "data setup time" is the time interval for the data at the buffer input to be ready and steady before the clock pulse is received.

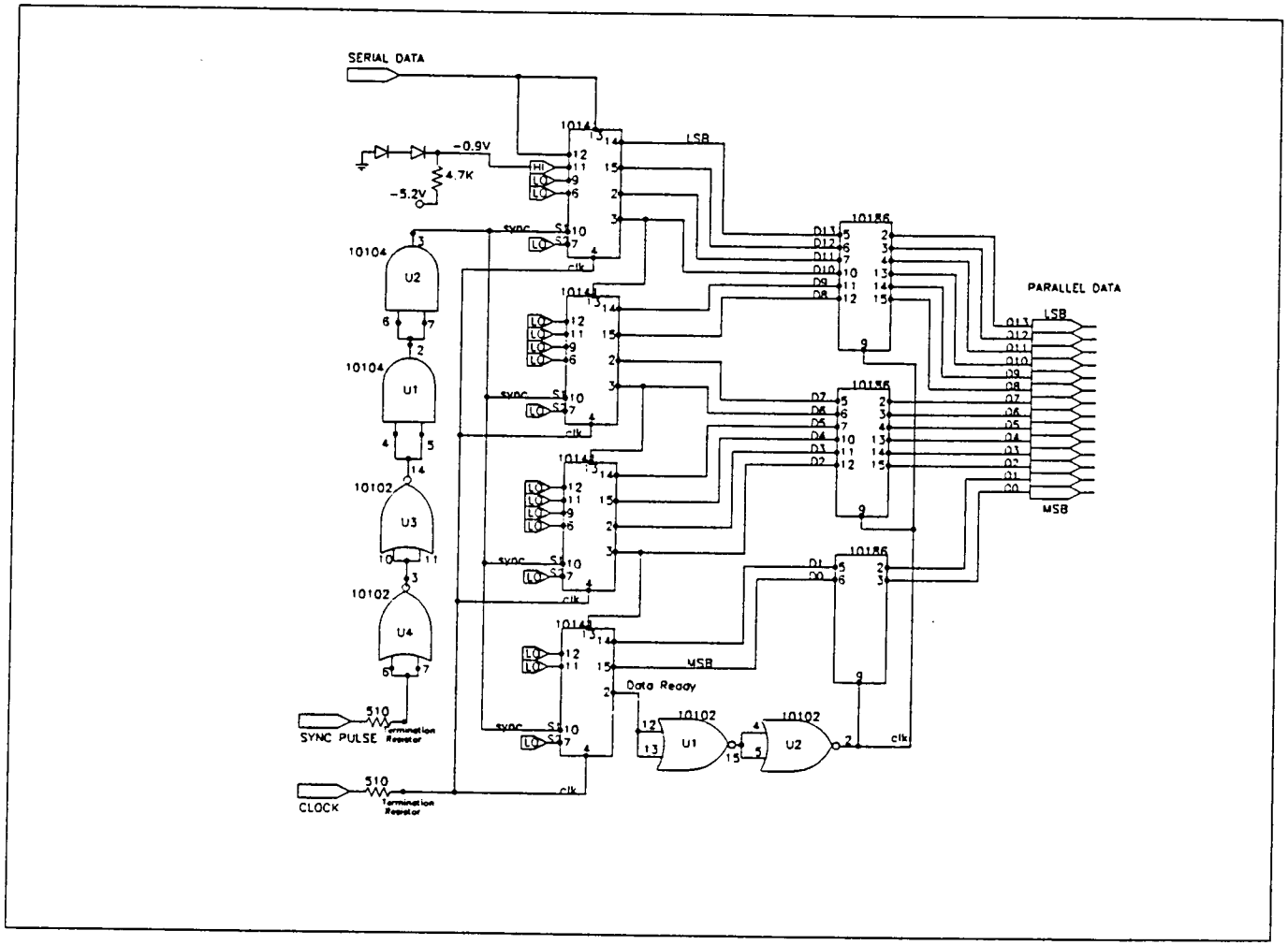
After this overview, we will now go into further details to understand the operation of the circuit. The detailed circuit of the receiver is shown in Figure 3.2.

B. SHIFT REGISTER

The function of a shift register is to receive the data from the serial input and to shift it right or left with a clock pulse. The operation modes of a shift register can be changed with two control inputs. The modes are "shift right", "shift left", "parallel entry" and "stop shift" as shown in Fig. 3.3. Four four-bit ECL shift registers were used in the circuit to convert serial data to 14-channel parallel data (the left-most devices shown as 10141 in Fig. 3.2).

The 70-MHz clock pulse sequence is provided from the transmitter (see Section II.A), because the frequencies used in the transmitter and the receiver must be exactly the same. Even a very small deviation in the frequency will cause the shift register to be triggered at the wrong times and shift the same bit twice or skip one bit.

The sync pulse coming from the transmitter is connected to one of the "control inputs" (S2) of the shift register. This low-level pulse with one clock period duration changes the operation mode of the shift register to "parallel entry" and initializes a new cycle for 14-bit data frame. When the following clock pulse is received, the parallel entry data is transmitted to the output. The first bit of the parallel entry data (Q0) is the most



*pull-down resistors are not shown for convenience

Figure 3.2. Receiver Circuit

S1(low)	S2(sync pulse)	OPERATION MODE
L	L	Parallel Entry
L	H	Shift Right
H	L	Shift Left
H	H	Stop Shift

Figure 3.3 The Operation Modes of the Shift Register.

recent bit of the serial data which is the first bit of the following 14-bit sequence. The second bit (Q1) is the "data ready strobe" (which is a logic "1") and the others are "0". To analyze the circuit more closely, assume that a logic "1" has appeared on the "data ready" line. On the next clock edge, the first bit of the data frame is entered into Q0 and a logic "1" into Q1 of the first register. All other outputs are loaded with logic "0"s. As more clock pulses occur, data are shifted in serially and the data ready line remains LOW until fourteen data bits are stored. At that point, the data ready line goes HIGH, indicating that the parallel data are ready and triggers the buffer. The cycle repeats every 200 ns.

C. BUFFER

The purpose of the buffer is to sample the data from the shift register output with the rising-edge of the clock pulse and to hold the voltage constant at the buffer outputs. The changes that occur at the input will not affect the output at any other time. Three hex, type-D, master-slave flip-flops are used for the purpose (shown as 10186 devices in Fig. 3.2).

The trigger pulse that triggers the flip-flops is the "data ready" strobe from the shift register. When 14 parallel data bits are stored, the "data ready" strobe reaches the "data ready line" and triggers the flip-flops. The parallel data are ready and stable at the output of the buffer for 200 ns. This is the final parallel output of the receiver subsystem.

D. DELAY CIRCUIT

NOR-gates are used to introduce delays in two different locations. The propagation delay of an ECL NOR-gate is typically 2 ns. Rise and fall time of the registers are 3.3 ns for the worst case condition and data setup time for the 10186 flip-flops is 2.5 ns. So, the worst case condition will require a 5.8 ns delay to trigger the flip-flops. As will be explained later, experimental testing showed that two NOR-gates are sufficient to provide required delay. (The specifications of the 10186 device and NOR-gates are given in Appendix A.)

The other requirement for a delay was for the sync pulse. The shift register must enter into its "parallel entry" mode one clock period later than the counter in the transmitter. When the 14th bit of the serial data is being sent, the counter in the transmitter goes into "parallel entry" mode but shift register should still remain in "shift right" mode to store the last bit. The next clock pulse will load the counter with the address of "0000" and the first bit of the following sequence will be sent. Now the register is ready for a parallel data entry. Experimental testing showed that for 70 MHz, two NOR-gates introduced enough delay. But, as will be explained in the Test and Evaluation chapter, if

the bit rate is reduced, the timing of the sync pulse must be changed and the delay time should be recalculated.

E. SUMMARY

In this chapter, the receiver has been discussed functionally followed by further details of the operation of the circuitry. The next chapter will discuss the test procedures and the measurements made to evaluate the correct operation. Some recommendations for further study will also be given at the end of the chapter.

IV. TEST AND EVALUATION

A. INTRODUCTION

The 14-channel parallel data with a bit rate of 5 Mbps were provided by a 14-bit analog-to-digital converter. The specifications of the ADS-944 Datel A/D Converter are presented in Appendix B. The parallel outputs of the converter were connected to the transmitter. The problem was to find a convenient 14-bit digital-to-analog converter to convert the digital data at the output of the receiver back into an analog signal. A D/A converter with an enough speed (5 MHz) was not available. The D/A converters on the market were too slow to meet the requirements. So, the digital data that were applied to the transmitter and that were taken at the output of the receiver were measured and compared manually. A block diagram of the test equipment and the necessary inter-connections are shown in Fig. 4.1.

B. A/D CONVERTER SETUP

An analog-to-digital converter is a device which converts the analog signal that is present at the input to a digital signal. The binary value of the digital signal corresponds to a predetermined level of the analog signal. This particular A/D converter, which is used in front of the transmitter, has an accuracy of 152.6 μV/bit. This means that increasing the analog input signal by 152.6 μV will cause summing up the digital output with a binary "1".

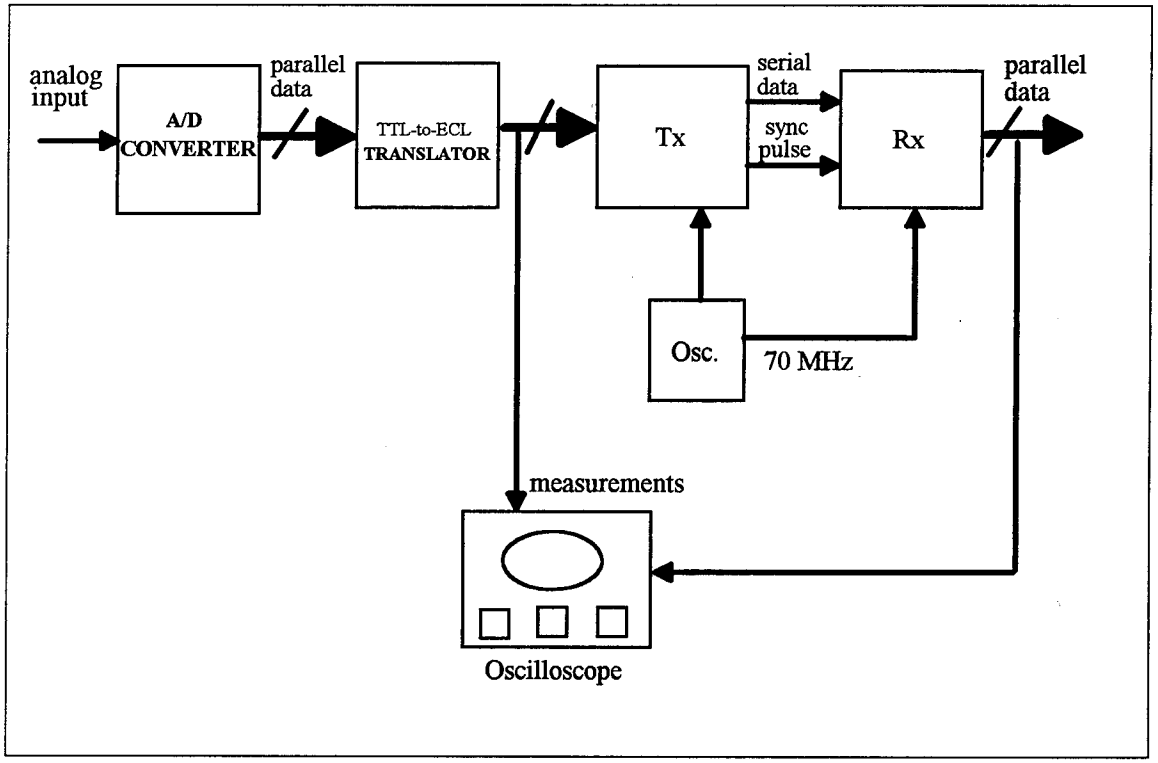
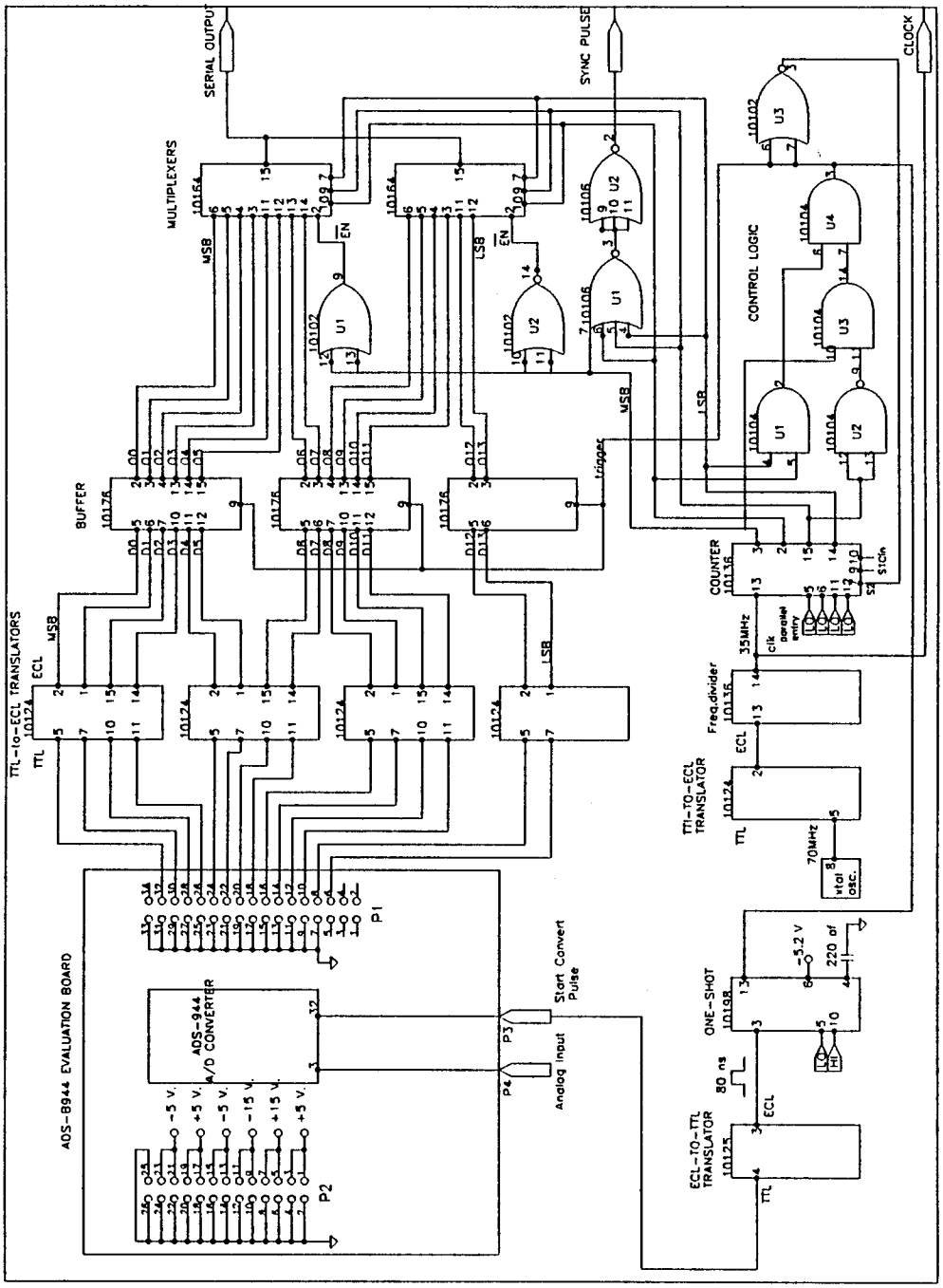


Figure 4.1. Block Diagram of the Test Equipment.

The conversion of the data is initiated by the rising edge of the "start convert pulse" which is generated by the control logic. This pulse is also used to trigger the buffer (see Fig. 4.2 for schematic diagram of the test circuit). But the requirement for the start convert pulse width is that it be between 40 ns and 80 ns or between 130 ns and 160 ns. So, a monostable multivibrator (one-shot) was used to generate this pulse width (see the 10198 device in Fig. 4.2). The control logic triggers the monostable multivibrator and a positive pulse with a pulse width of 80 ns is generated at its output. Since the output pulse has an ECL level, an ECL-to-TTL translator (see the 10125 device in Fig. 4.2) is used to translate the output to TTL level.

At the time t(0), the "start convert" pulse goes high (see the upper trace in Fig. 4.3) and initiates the data conversion. The pulse width of the "start convert" pulse is typically 80 ns. The previous parallel data at the output of the converter (see lower trace in Fig. 4.3) is valid for 120 ns after the rising edge of the "start convert" pulse. Due to a mismatch of propagation delays inside the converter, it is not guaranteed that the digital output data will be stable until 40 ns later (maximum value is 50 ns). Typically 160 ns after the rising edge of the "start convert" pulse, the new parallel data output will be valid at the output of the converter and will remain valid for 160 ns. The cycle repeats every 200 ns. The buffer can be triggered to take the parallel data from the output of the converter any time during the time interval that begins 40 ns before the "start convert" pulse and lasts until 120 ns later. For this thesis design, the rising edge of the "start convert" pulse is used for this purpose.



*pull-down resistors are not shown for convenience

Figure 4.2. Test Circuit

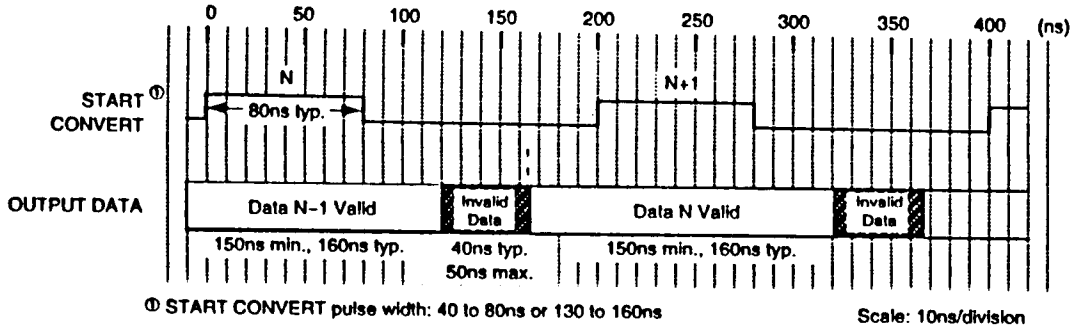


Figure 4.3. Timing Diagram of the A/D Converter [From Ref. 2].

Four TTL-to-ECL translators were used to convert the parallel data to ECL logic level (see the leftmost 10124 devices in Fig. 4.2). The output of the translators were connected to the buffer. The speed of the A/D converter is 5 MHz which allows a 200 ns period for sending 14-bit data with a bit rate of 70 Mbps.

C. THE NECESSITY OF THE SYNC PULSE

The requirement for using a synchronization pulse to synchronize the data manipulations in the transmitter and receiver forces us to use a separate link between the transmitter and the receiver which is undesirable. The "data ready line" in the receiver could be used to change the mode of the shift register to "parallel entry". In that case it would be possible to receive the data in correct sequence, but we would never know which particular bit was the first and which was the last. For example, the shift register could change the mode to "parallel entry" at which time the fifth bit was being sent. Then we would receive the fifth bit as if it was the first.

So, even if the common clock pulse is combined with the data on the same transmission line, it is necessary to use a second line for a synchronization pulse. Some other techniques may be used to insert the sync pulse on the same transmission line, but this was not investigated in this thesis.

D. TEST PROCEDURES

The buffer that is used in the receiver has a "data setup time" of 2.5 ns and a "data hold time" of 1.5 ns. The "data setup time" is the time interval for the data at the input of the device to be ready and steady before the clock pulse is received. The "data hold time" is the time for the data to stay stable after the clock pulse is received. So, stable data for 4 ns at the input of the buffer is needed for proper operation. This is the worst case calculation. The desired bit rate of 70 Mbps provided a period of 14.3 ns, which seemed to be enough time for the buffer, but the measurements showed that it was not. The only thing measured at the output of the buffer was a flickering data between "0" and "1". The delay times of the sync pulse and the data ready strobe were changed to test the circuit. But the result was the same. A stable and correct output was received only after the clock frequency was reduced to 39 MHz. The reason for the flickering data values was the setup and hold time of the buffer. So the hardware put a limit on the bit rate of the data. (The reason for the discrepancies between the specified performance and the measured performance of the buffers is unknown at the time of writing.) For a further development of the performance of the receiver, some faster buffer devices are required.

E. CONTROL LOGIC FOR DIFFERENT FREQUENCIES

For different bit rates, the arriving time of the sync pulse needs to be recalculated. For 70 Mbps, a delay of one period is provided by the propagation delays of the gates in the control logic and the delay circuit in the receiver. But for 39 Mbps, this is not a practical way to do it. The easier way is to generate the sync pulse when the counter is "0000" instead of "1101". A four-input NOR gate is used for this purpose (see the 10106 device in Fig. 4.2).

F. MEASUREMENTS

Since there was not a digital-to-analog converter available with enough speed to be used at the output of the receiver, a constant analog voltage level was applied as an input to the A/D converter to allow manual measurements. Several voltage levels were applied to evaluate the true transmission and reception. Only three of them will be presented here.

The A/D converter has an accuracy of 152.6 μV/bit as explained in Section IV.B. Hence the output of the A/D converter is very sensitive to the input voltage level. Neither batteries nor the zener diode voltage regulators can provide a voltage level with that stability. If the continuous conversion mode of the A/D converter is enabled during the manual measurements, we measure a stable voltage level for the first eleven bits (starting from MSB) of the parallel data, but a flickering data for the last three least significant bits. During the manual measurements, the trigger pulse which triggers the buffer was

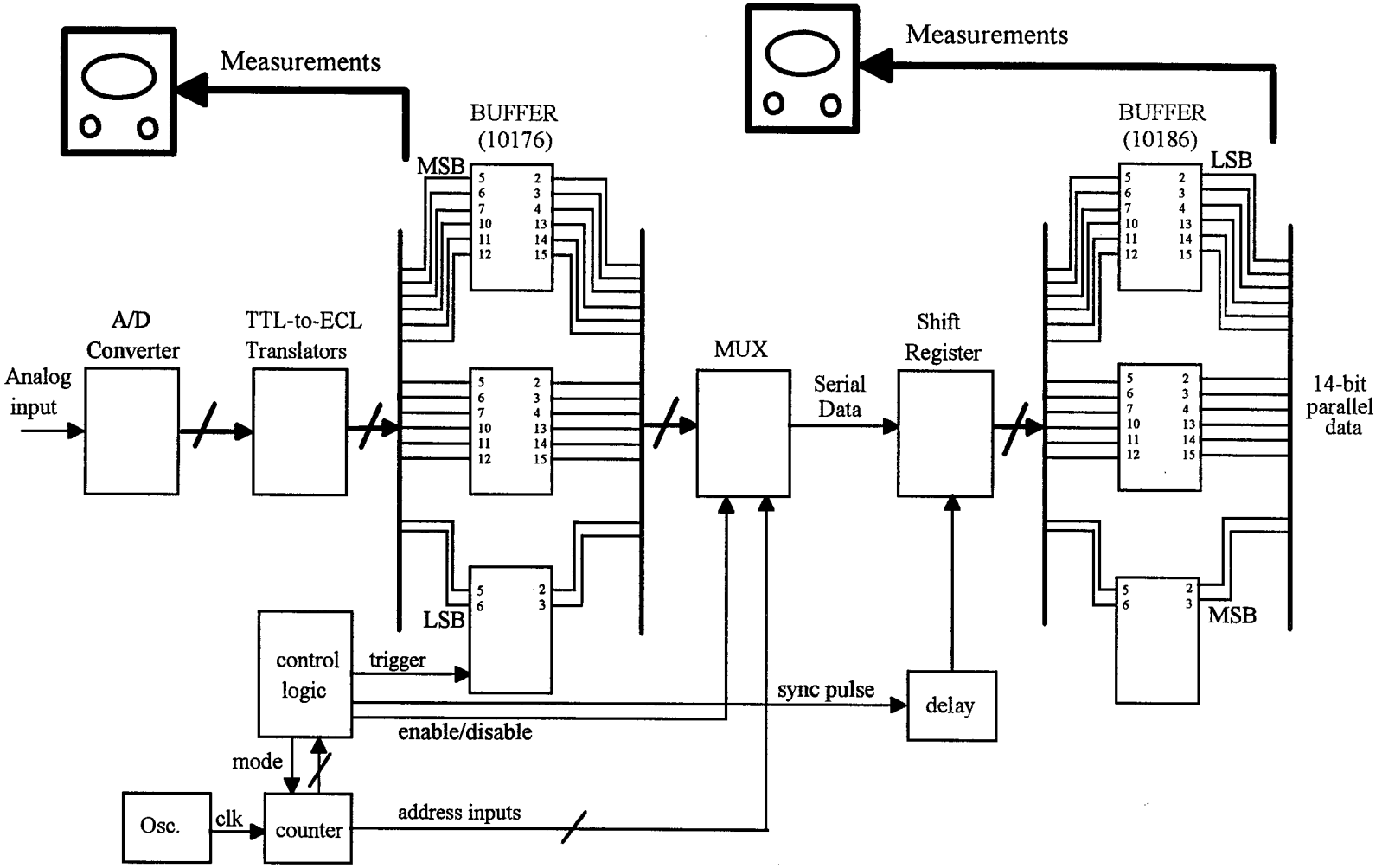


Figure 4.4. Evaluation Circuit.

disconnected before starting the measurements to make sure that all of the 14 parallel data bits at the input of the buffer are constant. The first analog voltage that was applied to the A/D converter was 1.0 V. This voltage level was converted to binary "10001000100011" and applied to the input of the buffer as parallel data. The "1"s and "0"s are ECL voltage levels which are -0.9 V and -1.7 V respectively. In Fig. 4.4, only the buffers in the transmitter and the receiver are detailed and their pin numbers, where the measurements were made, are given. The other circuit modules are left as a block diagram. The measurements were made at the input of the buffer in the transmitter and at the output of the buffer in the receiver. All the corresponding pins were the same, proving the true transmission and reception. The measured values are shown in Fig. 4.5.

G. SUMMARY

In this chapter, the test procedures of the design circuit have been introduced to the reader. The true transmission and reception of the 14 bits parallel data has been evaluated with the bit rate of 39 Mbps. The hardware limitations to achieve 70 Mbps transmission have also been discussed. Since there is not enough time to try different remedies, it has been left for further studies to achieve that bit rate. The setup of the test circuit with the A/D converter has been given. The necessity of the synchronization pulse and some explanations about it have been discussed. The control logic circuit for different clock frequencies is pointed out to try faster/slower bit rates. In the last section, some measured data are given as an example of true transmission and reception of the data. The

following chapter will conclude this thesis with the final results and give some possible remedies for further studies.

Analog Input Voltage	-1.0V		0.1V		1.0V	
Parallel Data	Input	Output	Input	Output	Input	Output
Q0	0	0	1	1	1	1
Q1	0	0	0	0	1	1
Q2	1	1	0	0	0	0
Q3	0	0	0	0	1	1
Q4	0	0	1	1	1	1
Q5	0	0	0	0	1	1
Q6	1	1	0	0	0	0
Q7	1	1	1	1	1	1
Q8	0	0	1	1	0	0
Q9	1	1	0	0	0	0
Q10	0	0	0	0	1	1
Q11	1	1	0	0	0	0
Q12	0	0	1	1	0	0
Q13	1	1	0	0	0	0

Note: "Input" stands for the input data to the buffer in the transmitter.
"Output" stands for the output data from the buffer in the receiver.

Figure 4.5. Measured Data.

V. CONCLUSION

A. SUMMARY OF RESULTS

This thesis accomplished the goal to serialize 14-channel digital data with a bit rate of 5 Mbps and to transmit them at 70 Mbps. The transmitter has a flexibility of changing the bit rate easily. The receiver, however, was not able to catch the data in correct sequence with 70 Mbps. The setup and hold time of the buffer in the receiver was not short enough for an incoming data with a period of 14.3 ns. The receiver received the data correctly below 39 Mbps and converted them back to parallel form. Above that bit rate, there was a flickering and unstable data at the output.

B. RECOMMENDATIONS FOR FURTHER STUDY

Some faster devices with a shorter setup and hold time can be investigated to accomplish 70 Mbps reception. For example, the MC10H176 from the MECL10KH family can be used instead of MC10176. The MC10H176 has a setup time of 1.5 ns and a hold time of 0.9 ns, whereas MC10176 has a 2.5 ns and 1.5 ns setup and hold time respectively, according to the specifications.

The clock pulse and the sync pulse can be embedded into the same transmission line with the serial data using some special techniques to avoid the need for extra links between the transmitter and the receiver. However, this will double the bit rate to 140 Mbps.

APPENDIX A

BRIEF DESCRIPTION OF THE DEVICES USED IN THIS THESIS

The following information is taken from Ref. 1.

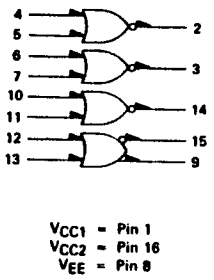
A. MC10102 QUAD 2-INPUT "NOR" GATE

P_D = 25 mW typ/gate (No Load)

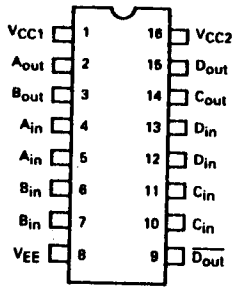
t_{pd} = 2.0 ns typ

t_r , t_f = 2.0 ns typ (20%-80%)

The MC10102 provides one gate with OR/NOR outputs.



Logic Diagram



DIP Pin Assignment

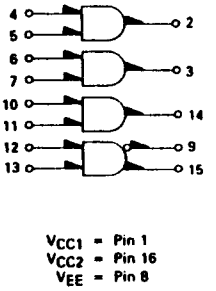
B. MC10104 QUAD 2-INPUT "AND" GATE

P_D = 35 mW typ/gate (No Load)

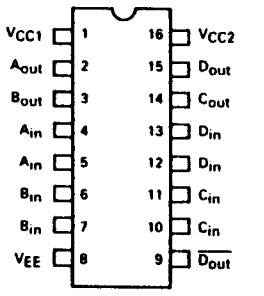
t_{pd} = 2.7 ns typ

t_r , t_f = 2.0 ns typ (20%-80%)

The MC10104 provides one gate with AND/NAND outputs.



Logic Diagram



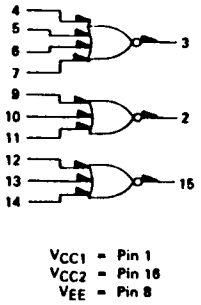
DIP Pin Assignment

C. MC10106 TRIPLE 4-3-3 INPUT "NOR" GATE

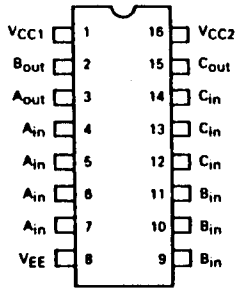
P_D = 30 mW typ/gate (No Load)

t_{pd} = 2.0 ns typ

t_r , t_f = 2.0 ns typ (20%-80%)



Logic Diagram



DIP Pin Assignment

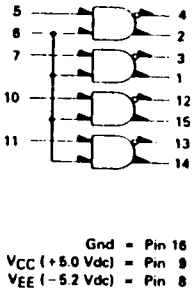
D. MC10124 QUAD TTL-TO-MECL TRANSLATOR

The MC10124 has TTL compatible inputs and ECL compatible outputs. Power supply requirements are ground, +5.0 V and -5.2 V.

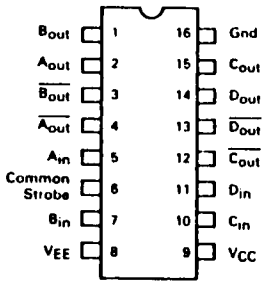
P_D = 380 mW typ/gate (No Load)

t_{pd} = 3.5 ns typ (+1.5 V in to 50% out)

t_r , t_f = 2.5 ns typ (20%-80%)



Logic Diagram



DIP Pin Assignment

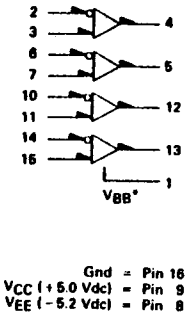
E. MC10125 QUAD MECL-TO-TTL TRANSLATOR

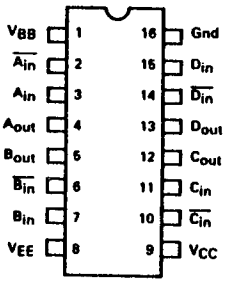
The MC10125 has ECL compatible inputs and TTL compatible outputs. Power supply requirements are ground, +5.0 V and -5.2 V.

P_D = 380 mW typ/gate (No Load)

t_{pd} = 4.5 ns typ (50% to +1.5 V out)

t_r , t_f = 2.5 ns typ (1.0 V to 2.0 V)





Logic Diagram DIP Pin Assignment

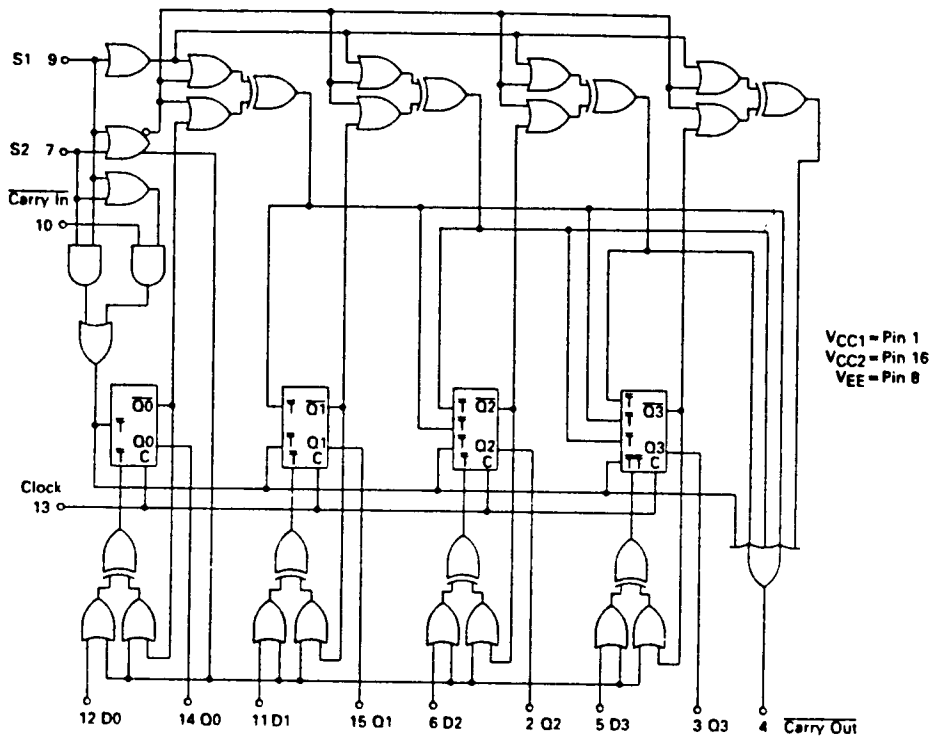
* V_{BB} to be used to supply bias to the MC10125 only and bypassed with 0.001 μF to 0.1 μF capacitor.

F. MC10136 UNIVERSAL HEXADECIMAL COUNTER

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. Three control lines (S1, S2 and Carry In) determine the operation mode of the counter. In the preset mode, a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2 and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when a preset code is present at the control inputs.

P_D = 625 mW typ/gate (No Load)

f_{count} = 150 MHz typ



NOTE: Flip-flops will toggle when all $\overline{T}$ inputs are low.

Logic Diagram

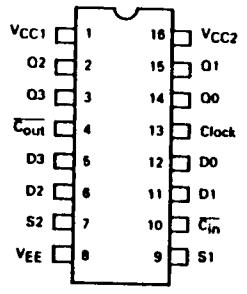
C_{in}	S1	S2	Operating Mode
ϕ	L	L	Preset (Program)
$\overline{L}$	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
ϕ	H	H	Hold (Stop Count)

Function Table

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{Carry\ In}$	Clock **	Q0	Q1	Q2	Q3	$\overline{Carry\ Out}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	H

ϕ = Don't care.
* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

Sequential Truth Table



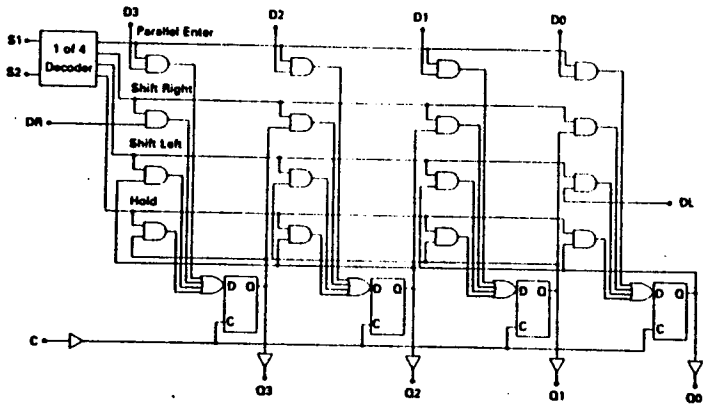
DIP Pin Assignment

t_{pd} = 3.3 ns typ (C-Q)
7.0 ns typ (C-C_{out})
5.0 ns typ (C_{in}-C_{out})

t_r , t_f = 2.0 ns typ (20%-80%)

G. MC10141 FOUR-BIT UNIVERSAL SHIFT REGISTER

The MC10141 is a four-bit universal shift register which performs shift left, shift right, serial/parallel in and serial/parallel out operations. Inputs S1 and S2 control the four possible operation of the register. The flip-flops shift the information on the positive edge of the clock. The four operations are stop-shift, shift left, shift right and parallel entry of data. The other six inputs are data inputs, four of which are for parallel entry data, one for shifting in from the left (DL), one for shifting in from the right (SR).



P_D= 425 mW typ/gate (No Load)

f_{shift}= 200 MHz typ

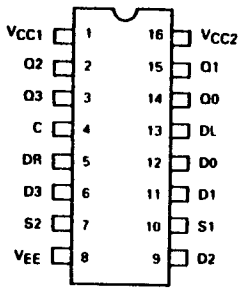
t_r , t_f= 2.0 ns typ (20%-80%)

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

*Outputs as exist after pulse appears at "C" input with input conditions as shown. (Pulse = Positive transition of clock input).



Logic Diagram

DIP Pin Assignment

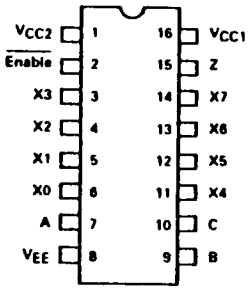
H. MC10164 8-LINE MULTIPLEXER

The MC10164 is a high-speed, low-power eight-channel data selector which routes data present at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs.

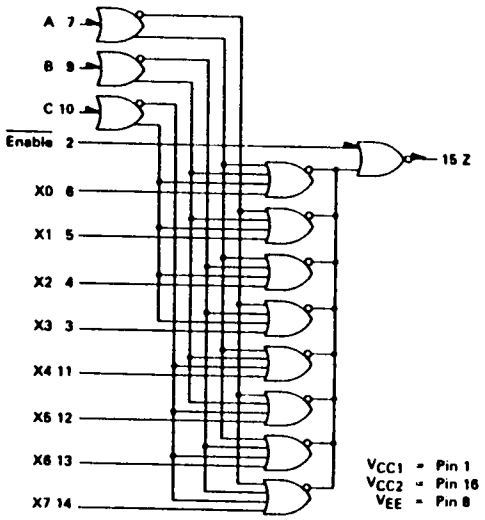
P_D = 310 mW typ/gate (No Load)

t_{pd} = 3.0 ns typ (Data to Output)

t_r , t_f = 2.0 ns typ (20%-80%)



DIP Pin Assignment



TRUTH TABLE

	ADDRESS INPUTS			
ENABLE	C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	ϕ	ϕ	ϕ	L

ϕ = Don't Care

Logic Diagram

I. MC10176 HEX "D" MASTER-SLAVE FLIP-FLOP

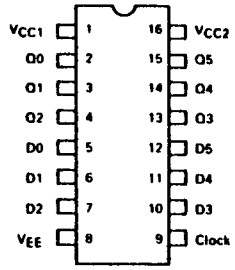
The MC10176 contains six high-speed, master-slave, type "D" flip-flops. Clocking is common to all six flip-flops. Data are entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going clock transition. Thus, outputs may change only on a positive-going clock transition. A change in the information present at the data (D) input does not affect the output information any other time due to

the master-slave construction of this device.

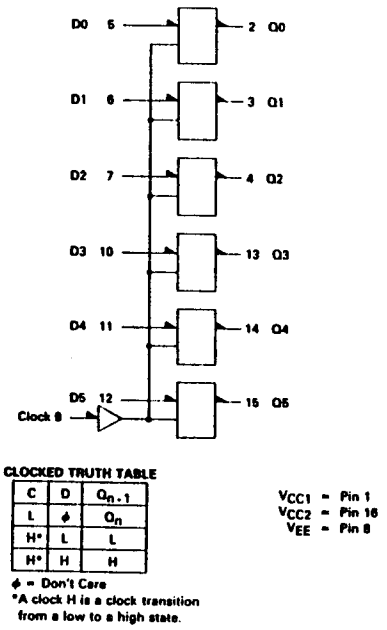
P_D = 460 mW typ/gate (No Load)

f_{toggle} = 150 MHz typ

t_r , t_f = 2.0 ns typ (20%-80%)



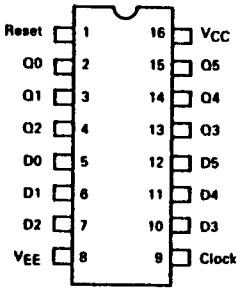
DIP Pin Assignment



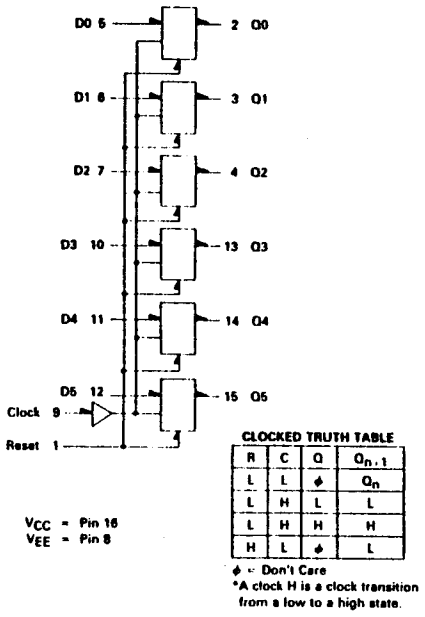
Logic Diagram

J. MC10186 HEX "D" MASTER-SLAVE FLIP-FLOP/WITH RESET

The MC10186 has the same features as the MC10176 except a reset input.



DIP Pin Assignment



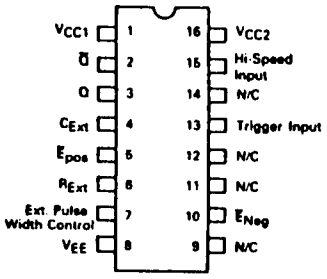
Logic Diagram

K. MC10198 MONOSTABLE MULTIVIBRATOR

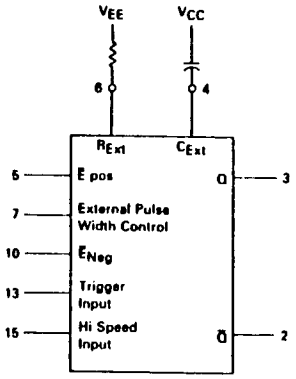
The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges. The pulse width is controlled by an external capacitor and resistor. The minimum pulse width that can be reached is 10 ns.

P_D = 415 mW typ/gate (No Load)

t_{pd} = 4.0 ns typ trigger input to Q



DIP Pin Assignment



VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8

TRUTH TABLE

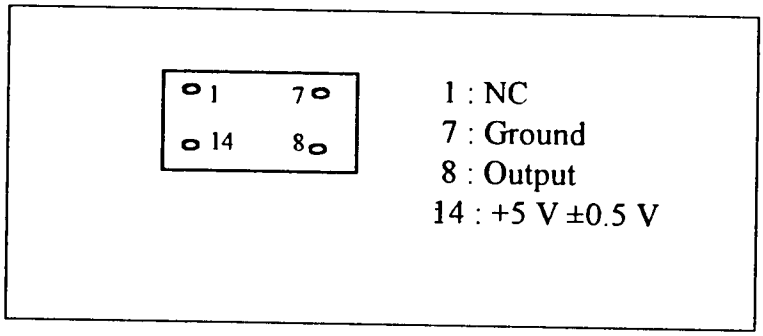
INPUT		OUTPUT
E_{Pos}	E_{Neg}	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled

Logic Diagram

L. 70 MHZ CRYSTAL OSCILLATOR

The output voltage levels are 0.5 V for a Low level and 2.4 V for a High level.

t_r , t_f = 5 ns



Dip Pin Assignment

APPENDIX B

ADS-944 ANALOG-TO-DIGITAL CONVERTER

This appendix describes the operation of the ADS-944 A/D converter. This information is taken from Ref. 2 and Ref. 3.

A. INTRODUCTION

The ADS-944 A/D converter is a 14-bit resolution, high speed analog-to-digital converter. The sampling rate is 5 MHz. The ADS-944 can sample input signals up to Nyquist frequencies. The digital input and output signals are TTL level.

Power supplies of ±15 V, +5 V and -5.2 V are required for operation. The analog input signal is bipolar with a range of ±1.25 V. The simplified block diagram is shown in Fig. B.1. An external calibration is not needed; if it is desired for some reason, the device's "small initial offset" and "gain errors" can be reduced to zero. For calibration procedures, refer to Ref. 2.

The ADS-B944 evaluation board was used to operate the ADS-944. The pin diagram of the ADS-944 A/D converter and the connectors on the ADS-B944 evaluation board are shown in Tables 1-3. The output coding of the converter and a brief explanation of the "start convert pulse" will follow the diagrams. The functions of the jumpers on the evaluation board will also be presented in the following sections. For further details of the converter, refer to Ref. 2.

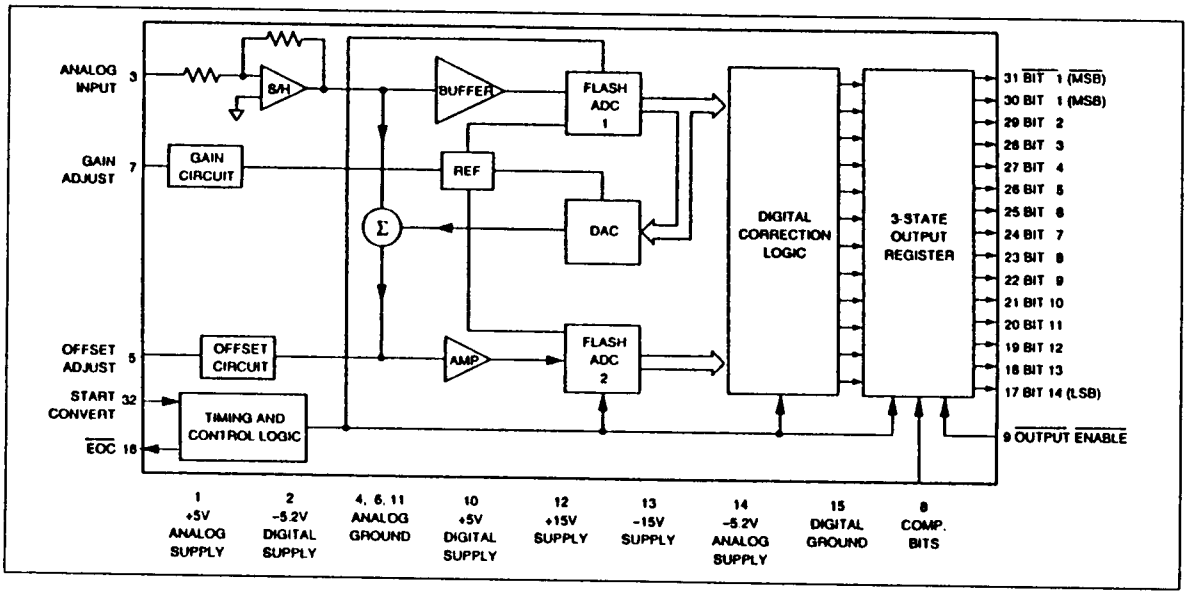


Figure B.1. Simplified Block Diagram of The ADS-944 A/D Converter [From Ref. 2].

B. PIN DIAGRAM OF THE CONVERTER AND THE CONNECTORS

PIN	FUNCTION	PIN	FUNCTION
1	+5V Analog Supply	32	Start Convert
2	-5.2V Digital Supply	32	Bit 1 (MSB)
3	Analog Input	30	Bit 1 (MSB)
4	Analog Ground	29	Bit 2
5	Offset Adjust	28	Bit 3
6	Analog Ground	27	Bit 4
7	Gain Adjust	26	Bit 5
8	Comp.Bits	25	Bit 6
9	Output Enable	24	Bit 7
10	+5V Digital Supply	23	Bit 8
11	Analog Ground	22	Bit 9
12	+15V Supply	21	Bit 10
13	-15V Supply	20	Bit 11
14	-5.2V Analog Supply	19	Bit 12
15	Digital Ground	18	Bit 13
16	$\overline{EOC}$	17	Bit 14

Table 1. I/O Connections of ADS-944 [From Ref. 2].

PIN	COLOR	FUNCTION	PIN	COLOR	FUNCTION
34	Yellow	Bit 1 (MSB)	33	Orange	Digital Ground
32	Red	Bit 1 (MSB)	31	Brown	Digital Ground
30	Black	Bit 2	29	White	Digital Ground
28	Gray	Bit 3	27	Violet	Digital Ground
26	Blue	Bit 4	25	Green	Digital Ground
24	Yellow	Bit 5	23	Orange	Digital Ground
22	Red	Bit 6	21	Brown	Digital Ground
20	Black	Bit 7	19	White	Digital Ground
18	Gray	Bit 8	17	Violet	Digital Ground
16	Blue	Bit 9	15	Green	Digital Ground
14	Yellow	Bit 10	13	Orange	Digital Ground
12	Red	Bit 11	11	Brown	Digital Ground
10	Black	Bit 12	9	White	Digital Ground
8	Gray	Bit 13	7	Violet	Digital Ground
6	Blue	Bit 14 (LSB)	5	Green	Complement (Input)
4	Yellow	Clock (Output)	3	Orange	No Connection
2	Red	Latches $\overline{OE}$	1	Brown	EOC (Output)

Table 2. P1-connector, 34-Pin Terminal Strip DIP (Output Bits and Controlled Functions) [From Ref. 3].

PIN	COLOR	FUNCTION	PIN	COLOR	FUNCTION
2	Red	Digital Ground	1	Brown	+5V Analog
4	Yellow	Digital Ground	3	Orange	+5V Analog
6	Blue	Digital Ground	5	Green	+15V
8	Gray	Digital Ground	7	Violet	+15V
10	Black	Digital Ground	9	White	-15V
12	Red	Digital Ground	11	Brown	-15V
14	Yellow	Analog Ground	13	Orange	-5V Analog
16	Blue	Analog Ground	15	Green	-5V Analog
18	Gray	Analog Ground	17	Violet	+5V
20	Black	Analog Ground	19	White	+5V
22	Red	Analog Ground	21	Brown	-5V
24	Yellow	Analog Ground	23	Orange	-5V
26	Blue	Analog Ground	25	Green	Analog Ground

Table 3. P2-Connector, 26-Pin Terminal Strip DIP (DC supplies) [From Ref. 3].

C. THE OUTPUT OF THE CONVERTER

Pin 8 of the converter is connected to pin 5 of the connector P1 of the evaluation board through jumper 1. (For the schematic diagram of the test circuitry, see Fig. 4.2.)

When the JUMPER 1 is in position 1-2, the complement input of ADS-944 (pin 8) is connected to ground. Thus the output bits are not complemented (offset binary, which is the code that was used to test this thesis design). The MSB may be used to achieve two's complement coding (see Fig. B.2).

OUTPUT CODING						INPUT RANGE	BIPOLAR
MSB	LSB	MSB	LSB	MSB	LSB	±1.25V	SCALE
11 1111 1111 1111		00 0000 0000 0000		01 1111 1111 1111		+1.249847	+FS -1 LSB
11 1000 0000 0000		00 0111 1111 1111		01 1000 0000 0000		+0.937500	+3/4 FS
11 0000 0000 0000		00 1111 1111 1111		01 0000 0000 0000		+0.625000	+1/2 FS
10 0000 0000 0000		01 1111 1111 1111		00 0000 0000 0000		0.000000	0
01 0000 0000 0000		10 1111 1111 1111		11 0000 0000 0000		-0.625000	-1/2 FS
00 1000 0000 0000		11 0111 1111 1111		10 1000 0000 0000		-0.937500	-3/4 FS
00 0000 0000 0001		11 1111 1111 1110		10 0000 0000 0001		-1.249847	-FS + LSB
00 0000 0000 0000		11 1111 1111 1111		10 0000 0000 0000		-1.250000	-FS
OFFSET BINARY		COMP.OFF.BIN.		TWO'S COMP.			

Figure B.2 Output Coding.

When the JUMPER 1 is in position 2-3, the complement input of ADS-944 (pin 8) is connected to pin 5 of the connector P1. Thus the user has the option of controlling the complement pin outside the evaluation board. Either logic "0" or "1" can be used. When logic "1" is applied, the output coding is "complementary offset binary".

For the detailed schematic diagram of the A/D converter, see Fig. B.3.

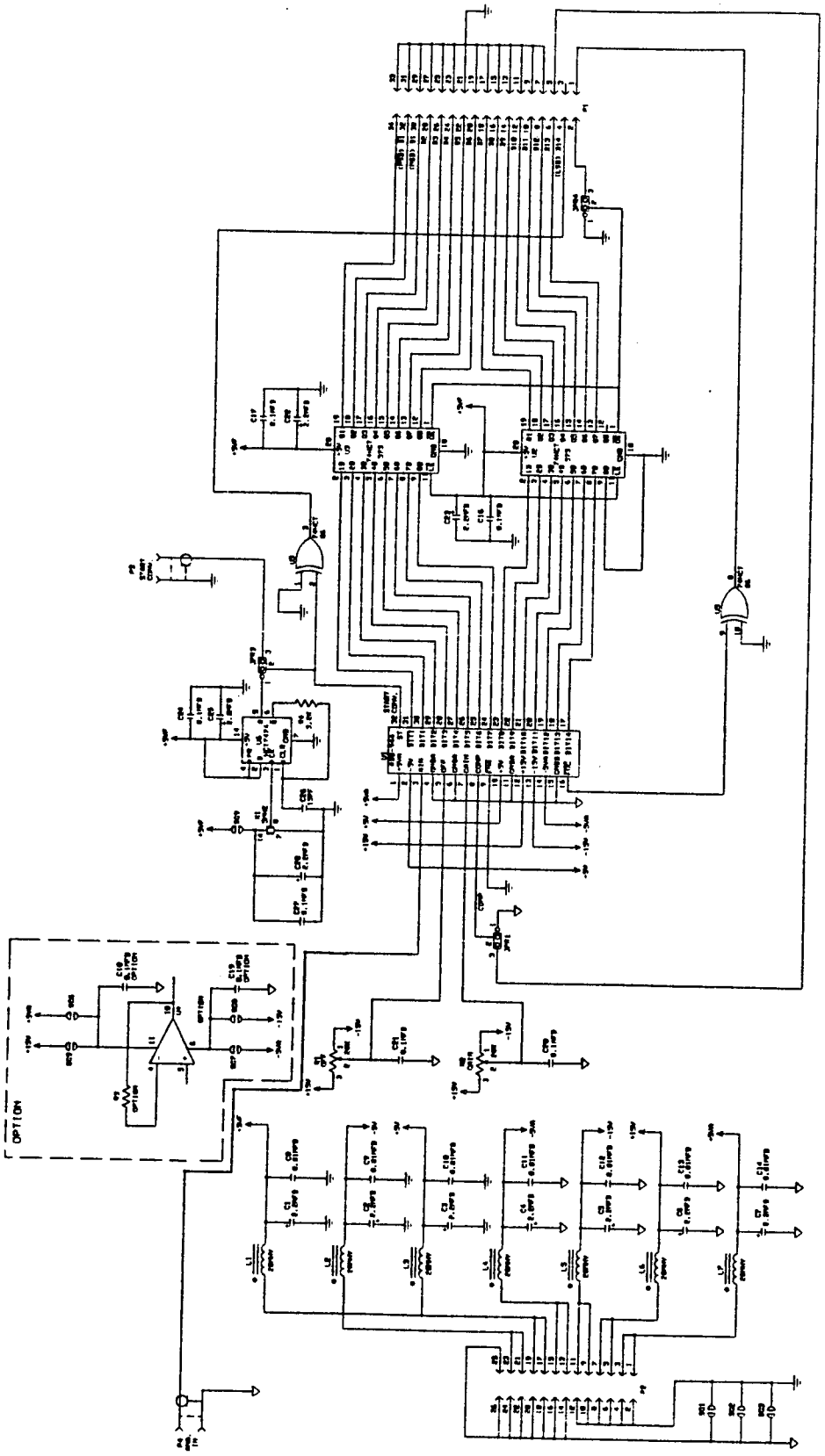


Figure B.3. Schematic of the ADS-B944 Evaluation Board.

D. START CONVERT PULSE

A start convert pulse with a maximum frequency of 5 MHz is needed to initiate the conversion.

When the JUMPER 2 is in position 1-2, the clock is provided internally by the use of a 5 MHz crystal oscillator.

When the JUMPER 2 is in position 2-3, the user has the option of using an external clock through the BNC connector labeled P3.

To test the thesis circuitry, an external clock is used. The clock, which also triggers the buffer, is generated by the control logic . This gives the user the flexibility to change the bit rate without causing any timing problems with the A/D conversion.

When the JUMPER 3 is in position 1-2, this setting makes the output bits of the A/D converter enabled all the time, by connecting the "output enable pin" of the latches in the evaluation board to ground (see 74HCT573 devices at the right-hand side of Fig.B.2).

When the JUMPER 3 is in position 2-3, the "output enable pins" of the latches are connected to pin 2 of connector P1. The user has the option of either enabling or disabling the output pins. The output pins are enabled all the time to evaluate the transmitter-receiver circuitry.

E. TIMING

The conversion of the analog signal is initiated by the rising edge of the start convert pulse. The conversion requires approximately 140 ns. The previous data are valid

at the output typically from 35 ns before the start convert pulse until 120 ns later. There is an unstable and invalid data for typically 40 ns (maximum 50 ns). After that, the data of the next cycle will be valid. For a detailed timing diagram, see Fig. 4.3.

Applying a start convert pulse while a conversion is in progress initiates a new and inaccurate conversion cycle.

APPENDIX C

EMITTER-COUPLED LOGIC FAMILY

This appendix contains useful information about working units of the "Emitter Coupled Logic" (ECL) family. The following information was taken from Ref. 1.

A. OVERVIEW

The ECL is today's fastest silicon-based digital logic. The MECL 10,000 series of the Emitter Coupled Logic was introduced by Motorola in 1971. MECL I, MECL II, MECL III, PLL (MC 12,000 series) and the new MECL10KH are the other ECL logic families which were all introduced by Motorola. The first two families are now obsolete, however. MECL III is a high power, high speed logic family compared with the others. Typical 1 ns edge speed and greater than 500 MHz flip-flop toggle rate make them useful for high speed test and communications equipment.

The MECL 10,000 series, which was employed in this thesis research, is for more general purpose applications and an easy-to-use logic family with typical propagation delays of 2 ns.

B. NEGATIVE/POSITIVE LOGIC

ECL family uses "positive logic" with NOR functions, whereas saturated logic families such as TTL use "negative logic" with NAND functions. It is not a complicated

issue to convert from one logic to another. Once the design is completed by using either of them, the user can easily switch between the two.

C. LOGIC LEVELS

The typical logic levels of the ECL families are a "-0.9 V" for logic High and a "-1.7 " for logic Low. The typical input and output voltage levels are shown on Table 4.

		INPUT		OUTPUT	
HIGH	maximum	(V_{IHmax})	-0.810 V.	(V_{OHmax})	-0.810 V.
	minimum	(V_{IHmin})	-1.105 V.	(V_{OHmin})	-0.900 V.
	threshold	(V_{IHAmin})	-1.105 V.	(V_{OHAmin})	-0.980 V.
LOW	threshold	(V_{ILAmax})	-1.475 V.	(V_{OLAmax})	-1.630 V.
	maximum	(V_{ILmax})	-1.475 V.	(V_{OLmax})	-1.650 V.
	minimum	(V_{ILmin})	-1.850 V.	(V_{OLmin})	-1.850 V.

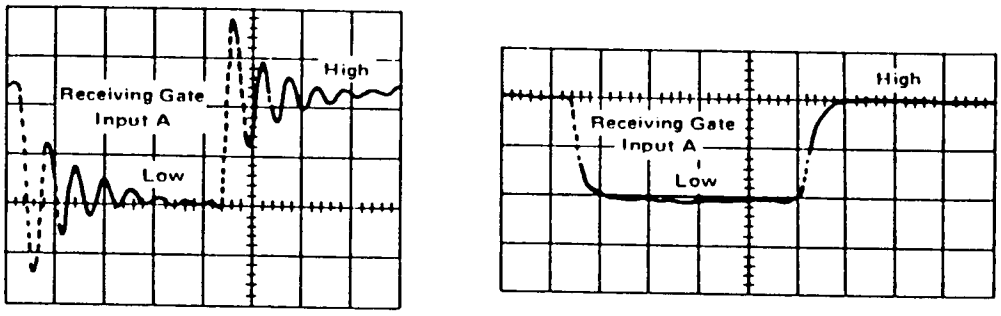
Table 4. ECL levels.

D. SOME BASIC CONSIDERATIONS

As the frequency and the edge speed of the IC devices goes up, time delays through interconnect wiring and the distortion due to reflections on signal lines become an issue to be considered. The possibility of crosstalk between adjacent signal leads and electrical noise generation are the other problems for high speed ECL families. The inter-

connect wiring time delays can be reduced only by reducing the length of the inter-connecting lines. A gate delay of 2 ns is introduced by every foot of wiring.

The solution to prevent waveform distortion due to line reflections is to employ transmission-lines and properly terminate each signal line. In this thesis design, transmission-line techniques were not used since the interconnection-wirings were not too long. But 100 Ω termination resistors were used to eliminate possible distortions. For a typical distortion due to line reflections, see Fig. C.1.



Unterminated Transmission Line Properly Terminated Transmission Line

Figure C.1. Distortion due to Line Reflections [From Ref. 1].

Either of the power supply levels, V_{CC} or V_{EE} can be used as ground. But for the best noise immunity, 0 V (ground) for V_{CC} and -5.2 V for V_{EE} was used. For the ECL-to-TTL and TTL-to-ECL translators, a +5 V voltage source is also needed. V_{EE} should not exceed beyond the limits of -4.68 to -5.72 V.

Because of the open-emitter outputs of ECL family, pull-down resistors are always required. 510Ω pull-down resistors to -5.2 V were used for this thesis design, which caused 9.7 mW power dissipation in the output transistors and 30.2 mW power dissipation

in the terminating resistors. The terminating resistors cause an additional 0.2 ns propagation delay per fanout load. 100Ω series damping resistors were also used to extend permissible lengths of unmatched-impedance interconnections (see Fig. B.2).

Most of the MECL logic circuits contain input pulldown resistors of a 50 kΩ between the input transistor bases and V_{EE}. So, unused inputs may be left unconnected and they are held sufficiently negative. The input pulldown resistors are not to be used as pulldown resistors for preceding outputs.

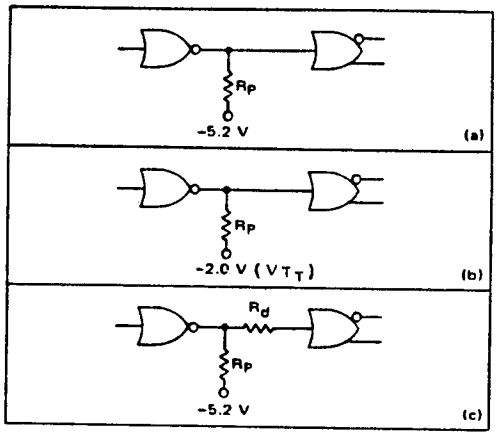


Figure C.2 Pulldown and Damping Resistor Techniques.

The MECL family does not operate properly when the inputs are connected to V_{CC} for a high logic level. A good design practice is to set a high level of -0.9 V below V_{CC} with a voltage divider, a diode drop, or an unused gate output. Two diodes in series were used for this thesis design. For low logic level input, the inputs may be left unconnected. Unused outputs draw no power and may be ignored.

Wire-OR capability of the ECL family allows direct connections of the output emitters together outside the packages. Although very little power supply noise is

generated, bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF capacitor between ground and -5.2 V line every four to six packages were employed for this design.

LIST OF REFERENCES

1. "Motorola MECL Device Data," Motorola, Inc., Phoenix, AZ, 1989.

2. Specification Sheet for ADS-944, 5 MHz, 14-bit, Sampling A/D Converter, Datel, Inc., Mansfield, MA, 1994.

3. Product Specification Sheet for ADS-B944 Evaluation Board, Code number 50721, Datel, Inc., Mansfield, MA, 1994.

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